MINIMIZING THE FIR FILTER AREA USED IN A FPGA POWER COMPUTING INSTRUMENT

Lecturer Eng. **Cătălin DAMIAN,** PhD[1], Assoc. Prof. Eng. **Cristian ZET** PhD[1],
Assist. Prof. Eng. **Elena DĂNILĂ**[1]

[1]Technical University „Gheorghe Asachi" of Iaşi,
Faculty of Electrical Engineering, Power Engineering and Applied Informatics

REZUMAT. Partea de instrumentaţie ocupă un loc important în orice domeniu. Lucrarea prezintă un instrument pentru măsurarea simultană a puterii active, reactive şi aparente implementat pe un circuit de tip arie logică programabilă. Implementarea fără optimizare a acestui instrument ocupă aproximativ 76% dintr-o arie logică de tip FLEX10K. Pentru a micşora spaţiul ocupat se încearcă o optimizare a blocurilor de filtrare. Metoda propusă se bazează pe scrierea coeficienţilor filtrelor ca sumă de puteri ale lui doi. Se obţine astfel o micşorare cu 10 % a spaţiului total ocupat.

Cuvinte cheie: instrumentaţie, arii logice, filtrare, calcul puteri

ABSTRACT. Instrumentation is essential in any domain. The paper presents an instrument for simultaneous active, reactive and apparent power measurement. The instrument is implemented on a field programmable gate array (FPGA) device. The instrument is fitting on 76% of total area of a FELX10K device if implemented without any optimization algorithm. To minimize the occupied area, an optimization for the filtering blocks is performed. The method consists in coding the filtering coefficients like sum-of-power-of-two (SOPOT) terms. The total area is with 10% less than the initial case.

Keywords: instrumentation, FPGA, FIR filtering, power computing

1. INTRODUCTION

Electric power monitoring is a very important task in many industrial applications. An efficient power management is the key to industrial progress. Traditional power measurements have been performed in both time and frequency domains. The time domain approach is the most efficient and the most accurate when root mean square (rms) and real power as well as their dependent quantities are computed. This is because the starting point for all digital methods are the voltage and current waveforms concurrently sampled at uniform intervals over one or more cycles [1]. The frequency domain can offer better results for distortion and harmonic influences but suffers when it deals with non-stationary signals.

There are classical instruments in which the power value results from physical phenomena or are computed by software algorithms using specialized signal processors. The power analyzer described here is based on a method that differs from those implemented in electrodynamic, electrostatic, thermal and Hall effect wattmeter's. The presented instrument offers better performances compared with software solutions with lower clock speeds (digital signal processor or microprocessor).

FPGAs are very powerful, relatively inexpensive and adaptable devices because their configuration is specified by an abstract description language. As their size, capabilities, and speed increased, they began to take over larger and larger functions, needed in modern instrumentation. By simultaneously performing all of the operations, FPGAs are also widely used for digital signal processing functions. Taking advantage of the re-configurability during system operation, an FPGA based design can become an In-System Programmable (ISP) [2] system. FPGAs are being used often instead of Application Specific Integrated Circuits (ASIC) and microprocessor because they offer higher performance, lower power consumption, short development time and reduced risk [3].

In [4] an analog-to-digital converter (ADC) using an intermediary conversion into Pulse Width Modulation (PWM) signal is presented. The digital part of the ADC has been economically implemented in Altera's Flex 10K device. Using this ADC, an instrument for simultaneous measurement of active, reactive and apparent power has been developed and presented in [5].

2. THEORY OF CALCULATION

This section describes the theory of real, reactive and apparent power, rms and power factor calculation. Definitions of various types of powers are found in the IEEE Standard Dictionary of Electrical and Electronics Terms [IEEE Std. 100-88] [6].

If v_t and i_t are periodic signals with period T, then the real power P is given as follows:

$$P = \frac{1}{T}\int_0^T i_t v_t dt \quad (1)$$

Reactive power is defined as a "quantity measured by a perfect watt-hour meter which carries the current of a single-phase circuit and a voltage equal in magnitude to the voltage across the single-phase but in quadrature therewith" [7]. At each frequency over its range, the voltage v_t leads the voltage in quadrate v_{t-90° by 90°. If v_{t-90° and i_t are periodic signals with period T, then the reactive power Q is given by:

$$Q = \frac{1}{T}\int_0^T i_t v_{t-90^\circ} dt \quad (2)$$

In this paper, the reactive power will be computed from the power triangle:

$$Q = \sqrt{S^2 - P^2} \quad (3)$$

where S is the apparent power, being calculated as product between the rms voltage V and the rms current I. The above equation (3) is true only for sinusoidal waveforms.

$$S = V_{rms} I_{rms} \quad (4)$$

The rms value is a basic measurement for an ac signal magnitude. It can be defined under practical or mathematical aspects. Practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Mathematically, the rms value of a continuous signal $V(t)$ is defined as:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt} \quad (5)$$

For time sampling signals, the rms calculation presumes squaring the signal, taking the average, and obtaining the square root:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)} \quad (6)$$

The power factor (PF) registers the ratio between the real power and the apparent power consumed by a load:

$$PF = \frac{P}{S} \quad (7)$$

3. POWER PARAMETERS COMPUTING INSTRUMENT

The arithmetical blocks are implemented into a Flex10k70 device using Quartus II development software. Figure 1 presents the architecture of this implementation. Digital components of the ADC are not presented here. Each voltage and current sample is sent to a Finite Impulse Response filter (*FIR*) for a primary filtration. The filter coefficients, generated using a FIR Compiler Software (MATLAB, GNU Octave or Scilab), are read from a ROM memory using a serial interface. This makes the filter programmable regarding the frequency response and its type.

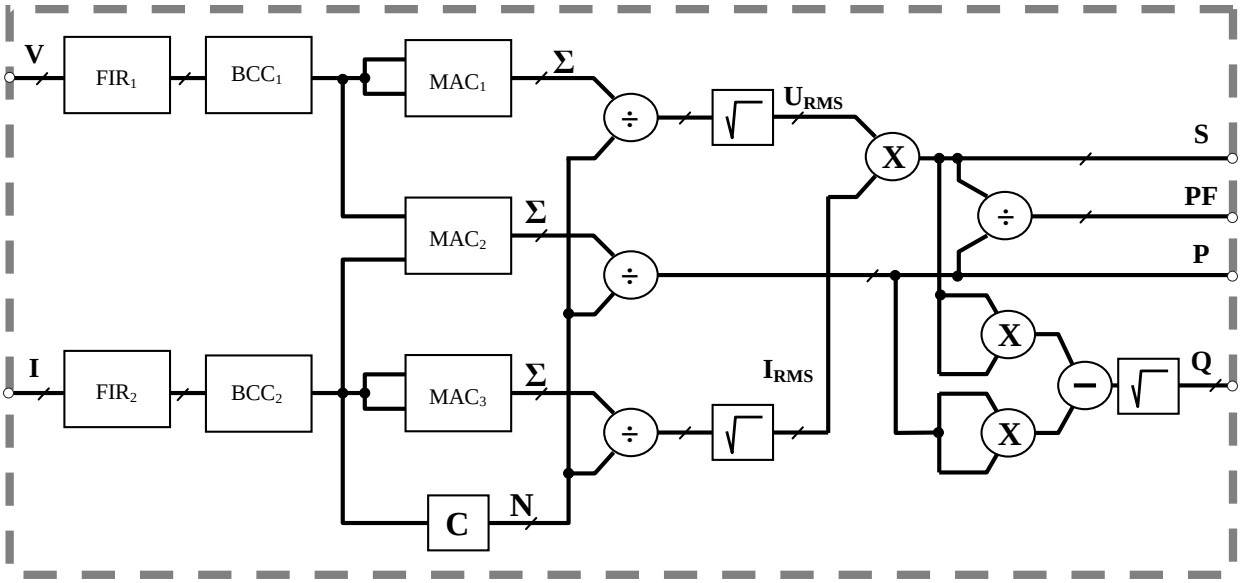

Fig. 1. Computing algorithm implemented in FPGA.

After the filtering stage, a binary code conversion is made (*BCC*). The ADC samples values are in offset binary code and for digital processing the data must be in two's complement format. To convert the format, the MSB of the each sample is inverted.

Next, the samples are multiplied and accumulated by a *MAC* (multiply and accumulate) block. These operations are synchronized with the other operations, on the basis of two general signals: clock and clear (Figure 2). The counter (*C*) detects the signal period generating the "clear" signal and the number of samples per period (*N*). Before clearing the MAC registers, the values are loaded into dividing blocks registers.

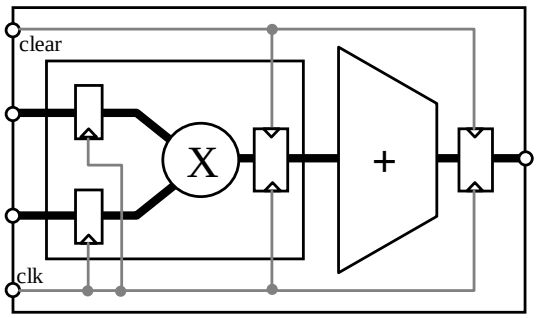

Fig. 2. Multiply and Accumulate Diagram.

MAC1 computes the ΣV^2, *MAC2* is computing the ΣVI and *MAC3* is computing the ΣI^2. A *MAC* entity for a 12 bits data occupies around 190 logical cells. This represents about 7% from the total number of Flex10k50 logic cells.

The square root operation is implemented in VHDL (VHSIC hardware description language) using a non-restoring algorithm [8]. This block occupies less than 100 logic cells from a total number of 2880. The computing time is around 1 μs.

Using other digital blocks (multiplying, dividing, subtracting) power factor, real, reactive and apparent powers are computed. These values can be directly displayed or used for controlling a process and/or sent to another device via a Serial Peripheral Interface Bus (SPI).

The presented instrument was implemented on an Altera's Flex10k50 FPGA device for single phase measurements. It fits 76% of logic cells without any resource sharing algorithm. A study for different Altera FPGA devices was performed and results are presented in Table 1.

Table 1

Fitting results for different Altera FPGA devices

Family	**FLEX10KE**	**Cyclone II**	**Stratix II**
Device	**EPF10K50SQC208**	**EP2C5T144C6**	**EP2S15F484C3**
Total logic elements	2197/2880 (76%)	323/4,608 (7%)	2%
Total registers	-	227	99
Total pins	36/147 (24%)	36/89 (40%)	36/343 (10%)
Total memory bits	128/40,960 (< 1%)	128/119,808 (< 1%)	128/419,328 (< 1%)
Embedded Multiplier 9-bit elements	-	16/26 (62%)	16/96 (17%)
Total PLLs	-	0/2 (0%)	0/6 (0%)

4. OPTIMIZING THE INSTRUMENT

In the previous implementation, the FIR filtering blocks are occupying about 50% of the total area on chip. In case of extending the instrument for three phase measurements, an optimization is required. The most valuable space-on-chip can be achieved by minimizing the filtering FIR blocks.

A FIR filter with constant coefficients is a linear time-invariant (LTI) digital filter. The output of a FIR filter of order or length *L*, to an input time-series *x[n]*, is given by a finite version of the convolution sum, namely:

$$y[n] = x[n] * f[n] = \sum_{k=0}^{L-1} f[k]x[n-k] \qquad (8)$$

where: $f[0] \neq 0$ through $f[L-1] \neq 0$ are the filter's *L* coefficients.

The Lth-order LTI FIR filter is graphically interpreted in Figure 3. It can be seen that this filter consists of a collection of a "tapped delay line", adders,

and multipliers. One of the operands presented to each multiplier is a FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure.

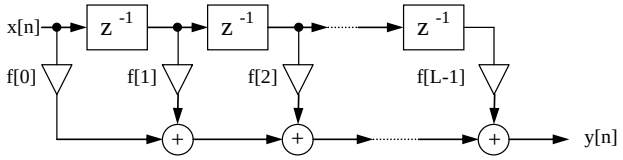

Fig. 3. Direct form FIR filter.

In order to implement a FIR filter into an FPGA device is necessary to scale the coefficients to integer values. If the coefficient values are integer's power-of-two, or a sum of power-of-two (SOPOT) with two or three terms, the multipliers can be replaced by shifters. In [9] and [10] are presented efficient FIR architectures based on theory of sums of two powers-of-two. Because of the errors introduced by the approximation of the filter's coefficients like a sum of two power-of-two terms, the purpose is to extend the algorithm to a sum of three power-of-two terms and to evaluate the resultant errors. The multiplier block from the Figure 3 can be replaced by shifters, as presented in Figure 4.

In this case each filter coefficient f[k] (1) can be implemented with SOPOT terms:

$$f[k] = \sum_{i=0}^{2} a_{i,k} \cdot 2^{b_{i,k}} \qquad (9)$$

where: $a_{i,k} \in \{-1,1\}$ and $b_{i,k} \in \{-t,\ldots,0,\ldots,u\}$; t and u determine the word length dynamic range of each filter coefficient. The larger the numbers t and u, the closer the SOPOT approximation will be to the original real number.

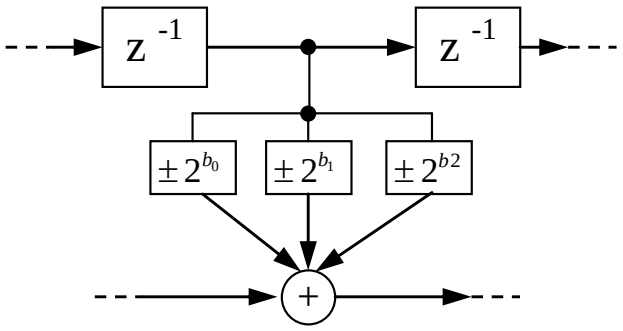

Fig. 4. Arithmetic unit of FIR filter with SOPOT type coefficient.

Based on the above algorithm, we carried out a study upon SOPOT approximation. Major differences were found between the performances obtained using the sum of three-power-of-two with respect to the sum of two power-of-two. Table 2 presents some examples and corresponding approximation errors.

Table 2

Example of two and three SOPOT terms

Integer	Two SOPOT	Three SOPOT
11	$2^3+2^1=10$ (10%)	$2^3+2^1+2^0=11$ (0%)
22	$2^4+2^2=20$ (10%)	$2^4+2^2+2^1=22$ (0%)
76	$2^6+2^4=80$ (5%)	$2^6+2^4-2^2=76$ (0%)

Some simulations have been performed using the Matlab software. Figure 5 shows the magnitude response of a 15 taps high-pass FIR filter. The coefficient set is scaled to integer with 8 bits resolution. The graph presents three magnitude responses, for three coefficient sets. It can be observed that for the two SOPOT terms, the rejection band is very different than the rejection band of real floating coefficient set.

There are situations when the codification of the coefficients by two SOPOT terms is more accurate in terms of filter's magnitude response, whereas the three SOPOT terms codification might be more efficient in terms of area occupied into FPGA.

Figure 6 presents a magnitude response of a 13 taps low-pass FIR filter. It can be observed that the rejection of the two SOPOT terms is better only in 0.8-0.85 normalized frequency band.

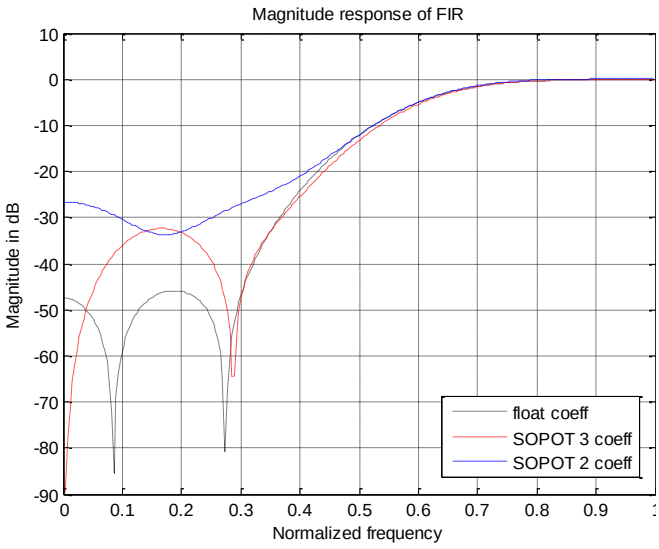

Fig. 5. Magnitude response for a high-pas FIR filter with different coefficient codification

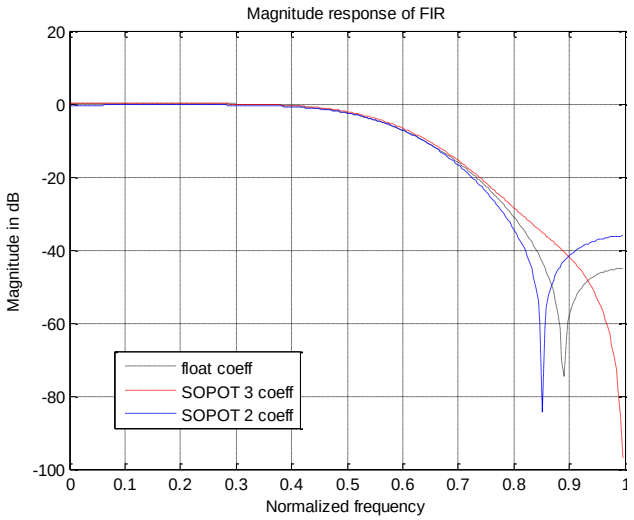

Fig. 6. Magnitude response for a low-pass FIR filter with different coefficient codification

Figure 7 shows a block diagram for a FIR filter using SOPOT type coefficients. The architecture proposed is appropriate for FPGA implementation with the remark that only minor modifications need to be accomplished in order to change this three SOPOT terms structure to a two SOPOT terms structure.

In the diagram, *D* represents a delay by one clock cycle block designed with D-type flip flops. *LSR* is a left shifting register designed from a parameterized combinational logic shifter mega-function provided by Quartus software tool. This register shifts the input bus with three different values. These values are represented by $b_{i,k}$ numbers. The inputs "*sign*" are "*logic zero*" if $a_{i,k}$ = +1 and "*logic high*" if $a_{i,k}$= -1. This input represents the sign of the shifted output value. In case of a zero coefficient, this direction it is not important because the result of the shifting operation will be zero in any case. The block "+" represents a bus signed adder.

The block diagram depicted in Figure 7 was implemented on an Altera's Flex10k device using Quartus II software. A seven tap 12 bits FIR filter using the present method and a traditional multiplier-based method were designed to evaluate the hardware requirements. The presented optimization method is reducing the area with 25%.

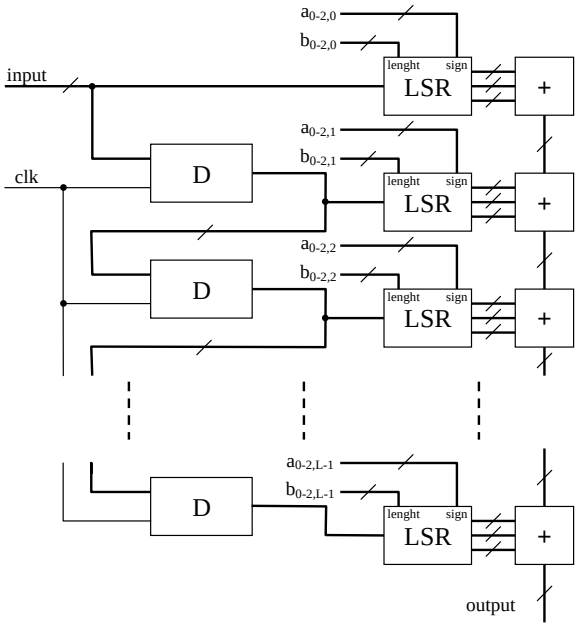

Fig. 7. Block diagram of FIR filter with three SOPOT terms type coefficient

5. CONCLUSIONS

This instrument can be used for power monitoring and can be easy interconnected with any other instrument or software tool that uses a digital interface. It provides real time information about power components like real power, reactive power, apparent power and power factor. The main advantages are related to small occupied area, fast computation and to the possibility of expanding to three phase systems.

A method for optimizing occupied area for a FIR type filter was presented. The optimizing results are presented in Table 3. If compared with the values presented in Table 1, some improvements regarding the total logic elements can be observed.

Table 3

Fitting results for different Altera FPGA devices

Family	**FLEX10KE**	**Cyclone II**	**Stratix II**
Device	**EPF10K50SQC208**	**EP2C5T144C6**	**EP2S15F484C3**
Total logic elements	1948/2880 (67%)	276/4,608 (5%)	2%
Total registers	-	208	91
Total pins	36/147 (24%)	36/89 (40%)	36/343 (10%)
Total memory bits	128/40,960 (< 1%)	128/119,808 (< 1%)	128/419,328 (< 1%)
Embedded Multiplier 9-bit elements	-	14/26 (54%)	14/96 (15%)
Total PLLs	-	0/2 (0%)	0/6 (0%)

The optimization is using a SOPOT algorithm. If the coefficient values are integer's power-of-two, or a sum of power-of-two with two or three terms, the multipliers can be replaced by shifters. For two SOPOT terms, the integer numbers can be coded with 10% errors and in case of coding with three SOPOT terms the errors can be minimized to zero.

ACKNOWLEDGMENT

This paper was supported by the project PERFORM-ERA "Postdoctoral Performance for Integration in the European Research Area" (ID-57649), financed by the European Social Fund and the Romanian Government.

BIBLIOGRAPHY

[1] **Yoon, W.Y., Devaney, M.,** "*Reactive power measurement using the Wavelet transform*", IEEE Transactions on Instrumentation and Measurement, vol. 49, pp. 246-252, 2000.

[2] **Goslin, G.R.,** "*A Guide to Using Field Programmable Gate Arrays (FPGAs) for Application-Specific Digital Signal Processing Performance*", XILINX, 1995.

[3] **Leong, P.,** "*Recent Trends in FPGA Architectures and Applications*", IEEE Computer Society, 2008

[4] **Zet, C., Damian, C., Foşalău, C.,** "*New type ADC using PWM intermediary conversion*", XIX IMEKO TC4, Iasi, Romania, Sept. 2007.

[5] **Damian, C., Zet, C., Fosalau, C., Cretu, M.,** "*Real, Reactive and Apparent Power Computing Using FPGA and PWM Intermediary Conversion*", XX IMEKO TC4, Florence, Italy, Sept. 2008.

[6] **Filipski, P.S., Baghzouz, Y., Cox, M.D.,** "*Discussion of power definitions contained in the IEEE dictionary*", IEEE Transactions Power Delivery, vol. 49, pp. 1237-1244, 1994.

[7] **Djokic, B., Bosnjakovic, P., Begovic, M.,** "*New method for reactive power and energy measurement*", IEEE Transactions on Instrumentation and Measurement, vol. 41, pp. 280-285, 1992.

[8] **Piromsopa, K., Aporntewan, C., Chongsatitvatana, P.,**"*An FPGA implementation of a fixed-point square root operation*", International Symposium on Communications and Information Technologies, pp. 587-589, 2001

[9] **Yeung, K. S., Chan, S. C.,** "*Multiplier-Less Digital Filters Using Programmable Sum-Of-Power-Of-Two (Sopot) Coefficients*", IEEE International Conference on Field-Programmable Technology, 78 – 84, 16-18 Dec. 2002.

[10] **Evans, J. B.,** "*An Efficient FIR Filter Architecture*", IEEE International Symposium in Circuits and Systems, 1993.

About the authors

Assist. Eng. **Cătălin DAMIAN**, PhD
"Gheorghe Asachi" Technical University of Iasi, Faculty of Electrical Engineering, Bd. Mangeron 23, 700050, Iasi, Romania
email:cdamian@ee.tuiasi.ro

Catalin Damian is a teaching assistant within the Faculty of Electrical Engineering, Department of Electrical Measurements and Materials, teaching courses and practical classes in "Digital Signal Processors", "Instrumentation for Environmental Measurements", "Operating Systems" and "Programming Computers an Programming Languages". In July 2009 he finished the Ph.D. stage sustaining the thesis with the title "Researches on the measurement techniques using digital signal processing" obtaining the Ph.D. degree in electrical engineering. He is the first author or co-author of 30 scientific papers, of which 8 are ISI proceedings.

Assoc. Prof. Eng. **Cristian ZET**, PhD.
"Gheorghe Asachi" Technical University of Iasi, Faculty of Electrical Engineering, Bd. Mangeron 23, 700050, Iasi, Romania
email:czet@ee.tuiasi.ro

Cristian Zet was born in Iasi, Romania in 1967. He received his diploma in engineering from the Technical University of Iasi, Faculty of Electronics and Telecommunications in 1992. He joined the Electrical Measurements Department, at The Faculty of electrical engineering in 1993. In 2002 he received the PhD from the Technical University of Iasi for his work in the field of data acquisition systems. Between 2002 and 2004 he joined the Material Research group at GSI Darmstadt for a postdoc grant. Presently he is associate professor and vice dean at the Faculty of Electrical Engineering, Technical University Gheorghe Asachi of Iasi.

Assis. Eng. **Elena DANILA**,
"Gheorghe Asachi" Technical University of Iasi, Faculty of Electrical Engineering, Bd. Mangeron 23, 700050, Iasi, Romania
email:danila_e@yahoo.com

Graduated at Faculty of Electrical Engineering, specialization Economic Engineering in Electrical, Electronic and Power Engineering. She is teaching practical classes in Energy Utilization, Optimal Energy Utilization, Low Voltage Utilities, Design of Low Voltage Wiring, Optimization of Power Consumption and is author or co-author of over 15 scientific papers.