DESIGN AND PERFORMANCE EVALUATION OF A LOW COST AUTOMATIC GAIN CONTROL CIRCUIT

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REZUMAT. Datorită perturbațiilor introduse de fading este nevoie de o continuă îmbunătățire a circuitelor de reglaj automat al amplificării AGC (Autimatic Gain Controller). Circuitele AGC au ca funcție principală obținerea unui nivel de semnal constant la ieşire indiferent de variația semnalului de intrare. Această variație a semnalului poate duce la pierderea informației sau la scăderea critică a performanței. În această lucrare este prezentată analiza, proiectarea şi evaluarea performanțelor unui circuit AGC cu buclă de reacție.

Cuvinte cheie: circuit de reglaj automat al amplificării, circuit, AGC, fading.

ABSTRACT. Due to the disturbances caused by the fading phenomenon (defined as the amplitude variation of received signal), there is a continuous need to improve the automatic gain control circuits (AGC). The main function of AGC circuits is to obtain a constant output signal level regardless of input signal variation. This variation can determine loss of information or critical decrease in the level of performance. This paper presents the design and performance evaluation of a feedback loop AGC circuit.

Keywords: Automatic Gain Controller, circuit, AGC, fading.

1. INTRODUCTION

The rapid development of communication systems also entailed the increased need for better selectivity and good control of the output signal level which became fundamental issues in the design of communication systems. Due to the disturbances caused by the fading (defined as variations in the amplitude of the received signal), there is a constant need to improve the automatic gain control circuits in order to acquire a constant output signal. Therefore, circuits have been designed, whose main function is to maintain a constant signal level at the output, regardless of the variations of the input signal of the system. The variations of the output signal could lead to the loss of data or to critical performance levels of the entire communication system. These circuits were described throughout the years as Automatic Gain Control (AGC) circuits.

The typical AGC circuits often have a low performance level in the case of parasitic oscillations in a wide frequency range. Therefore, the implementation of the circuits often entails the use of: multipliers, digital-analog converters and high speed comparators. The main objective of these circuits is to correct the variation of the input signal by properly adjusting the gain. The control signal is often acquired by means of a feedback loop [1]. The automatic gain control systems presented in the scientific literature [2]-[6] are constantly improved as communication systems become faster, more accurate and more complex. This paper consists in the analysis, design and performance assessment of a feedback loop AGC circuit using the Orcad simulation environment.

Thus in section II is presented a brief introduction regarding the AGC systems and in section III is presented the general structure of an AGC system with feedback loop. In section IV is presented the proposed AGC circuit at transistor level and is detailed the operating principle. Section V presents the simulations results in order to determine the level of performance. The paper ends with the conclusions section.

2. AGC SYSTEM THEORY

The scientific literature includes numerous theoretical descriptions of AGC systems, from non-linear approximations to multivariable analyses. Each model has its advantages and disadvantages but, when comparing the final results with the practical ones, several inconsistencies are detected (a high degree of inaccuracy). The general structure of an AGC system is presented in Figure 1.

The input signal is amplified by a variable gain amplifier (VGA), whose gain is controlled by an external signal VC. The VGA output can further be amplified in order to reach an adequate level of the VOUT external signal. The amplitude, frequency and modulations parameters of the output signal can be monitored by the detector; any unwanted component is filtered by a low pass filter (LPF) and subsequently compared with the reference signal. The result is then used to generate the control voltage VC which is further used to adjust the gain of the VGA [7].

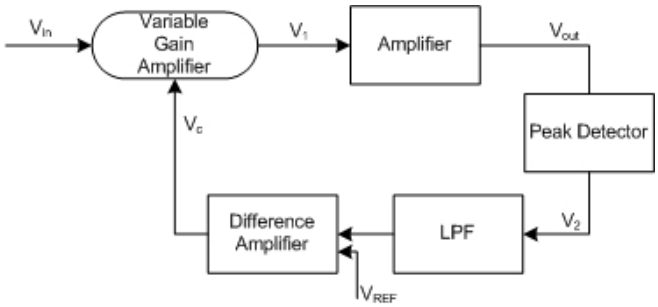

Fig.1. AGC general structure

The ideal transfer function of such a system is presented in Figure 2. For low input signals, the AGC circuit is in stand-by and the output is a linear function of the input and, when the output reaches a certain threshold value V_1, the system becomes operational and maintains a constant level of the output until a second value V_2 is reached. The AGC subsequently returns to its initial stand-by state in order to prevent the stability issues that may occur at high levels of gain [7].

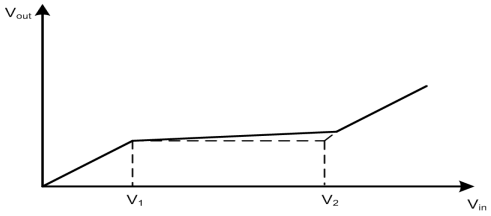

Fig. 2. The ideal transfer function of an AGC

3. AGC CIRCUIT WITH FEEDBACK LOOP

Figure 3 shows the block diagram of the AGC system. The circuit uses two envelope detectors, one for the positive alternation and another for the negative alternation of the input signal.

The signals from the two peak detectors (V_{peak_p} şi V_{peak_n}) pass through a low-pass filter. The control signal Vctrl from the feedback loop is obtained by means of an operational amplifier. At the positive input of the operational amplifier, a V_{set} signal is applied, which will set the amplitude level of the circuit output signal; meanwhile the negative inputs are applied to the two envelopes (negative and positive) detectors of the differential input signal.

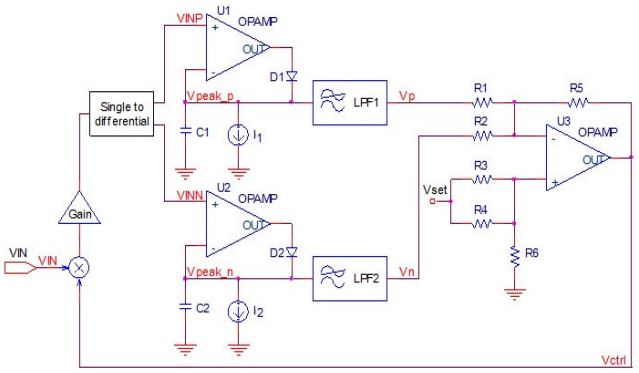

Fig. 3. AGC block diagram with feedback loop

Considering the circuit scheme, $R_1=R_2=R_3=R_4=R_5=R_6$ the control signal V_{ctrl} can be obtained using:

$$V_{ctrl} = (V_{set} - V_p) + (V_{set} - V_n) \quad (1)$$

The control signal Vctrl from the feedback loop and the input signal are then applied at the analog inputs of a multiplier which has a gain. The feedback loop ensures that, after the transitional regime ends, the inputs of the differential operational amplifier are equal:

$$V_{set} = V_p = V_n \quad (2)$$

In this case, according to equation (2), the control signal equals zero (V_{ctrl} = 0) which maintains a continuous amplitude of the circuit output signal at the desired amplitude V_{set}. Therefore, this circuit ensures that a constant amplitude output voltage is set by V_{set}.

4. PROPOSED AGC CIRCUIT

Figure 4 presents the proposed AGC circuit at the transistor level. For the implementation of the multiplier, a Gilbert cell is designed in order to achieve the multiplication of the differential input signal with the voltage control V_{crtl}. A common voltage mode V_{CM} of 3.5 V is overlapped over the control signal which is applied to the Gilbert cell. The second multiplier set of inputs are fitted with the differential test signal that can be an amplitude modulated signal designed to test the performance level of the proposed circuit. For common voltage mode reasons, a 1.5 V voltage is overlapped over the input signal. An amplitude modulated signal is designed from a harmonic sinusoidal signal with a

frequency of 1 MHz and 1V amplitude which is modulated over a signal with a frequency of 25 kHz and an amplitude of 45 mV.

The control signal V_{ctrl} is obtained using a difference operational amplifier which has as inputs the VP and VN signals from the two envelope detectors (designed using a OPA 358 circuit) and V_{set} which sets the output amplitude signal.

The VP and VN signals are then filtered using a low-pass filter which is designed using a 50 Ω resistor and a 40 nF capacitor. Operational amplifiers are powered at a continuous voltage of 3.33 V. The Gilbert cell is powered with a 5 V supply voltage and a 1mA current source. The assembly consisting in the C_{e1}, C_{e2} capacitors of 220 nF, the R_{l1}, R_{l2} resistors and the power-supply V_{REF}, are used in order to centre the output signal provided by the Gilbert cell on a common mode voltage of 1.5 V, necessary for the proper operation of the two envelope detectors. In order to eliminate the errors on the convergence of the static operation point (which occurred in the performed simulations) the linearization resistors: R_{l1}, R_{l2}, R_{l3}, R_{l4}, R_{l5}, R_{l6} were introduced. Figures 5 and 7 present the Gilbert circuit and the peak detector circuit.

The components that are included in the design of the automatic gain controller circuit were selected for economical reasons.

4.1. MULTIPLIER CIRCUIT

The balanced modulator (the mixer) is a circuit unit present in many blocks of radio receiving stations, and is used for the translation of the spectrums on the frequency axis.

Thus, the balanced modulator is a circuit that performs a linear modulation (simple frequency translation), providing an output signal in which a portion of the spectrum is missing:

-the spectrum of one input signal - simple balanced modulator (SBM);

-the spectrum of both input signals - double balanced modulator (DBM).

In order to implement the multiplier, a Gilbert cell is used as a double balanced modulator. Figure 5 presents the Gilbert cell circuit. The resistor R_3 100 kΩ, is used to transform the current cell output in voltage without the need of a current-voltage converter. The Resistor R_liniar is used to increase the linearity of the cell. The Gilbert cell has been implemented by using Philips BFR92A transistors from the PHIL_RF library.

If the Gilbert cell input signals, the carrier and the signal that is modulated have small amplitudes and can take both positive and negative values, the circuit performs a 4-quadrant multiplication.

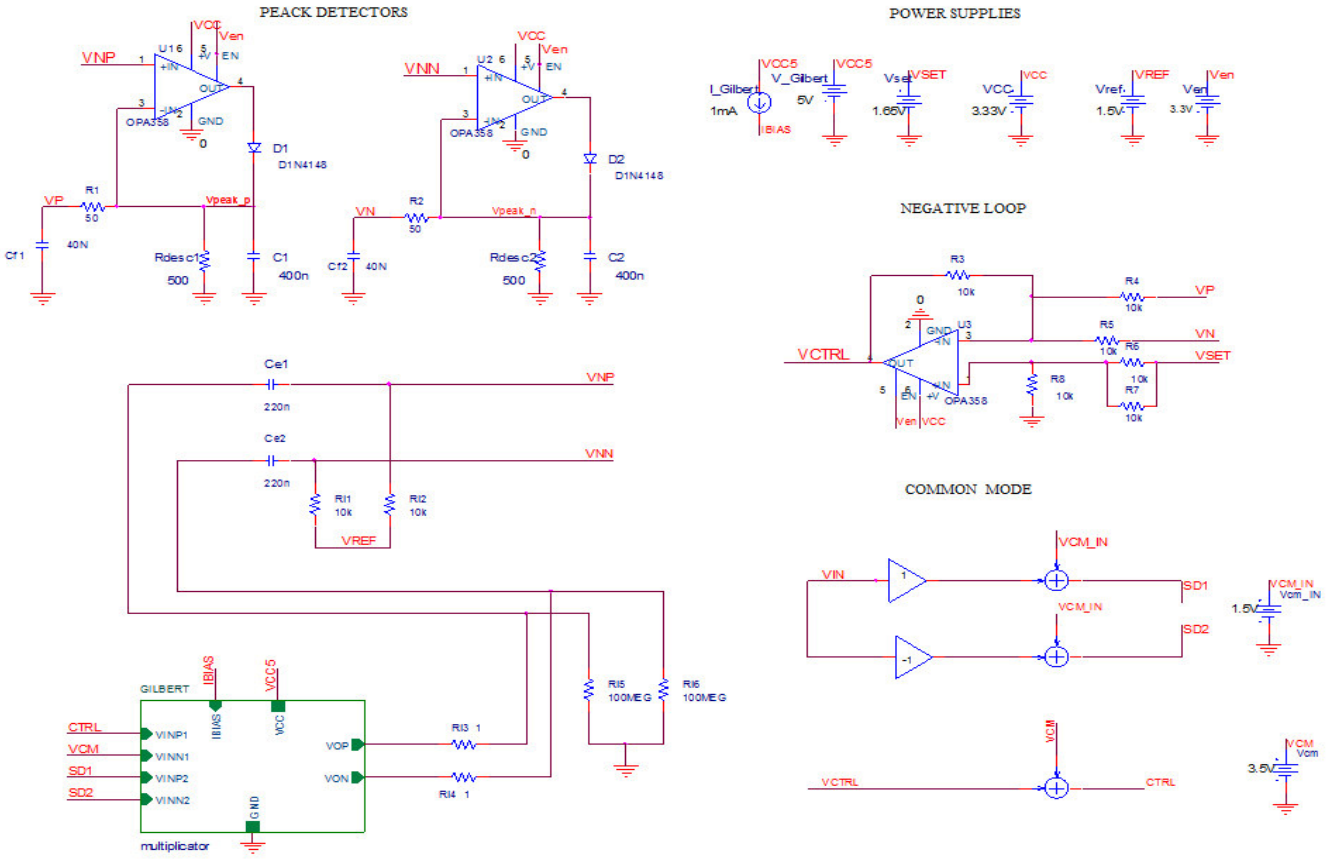

Fig. 4. AGC simulation circuit

In case the modulated signal amplitude is small, and the carrier signal has a relatively big amplitude, it can be observed that the spectrum of the output signal is missing the even components. The 4-quadrant analog multipliers are only developed as integrated circuits, as the transistors need to match perfectly.

A harmonic signal with a 100 kHz frequency and an amplitude of 5 mV overlapped with a common mode voltage of 1.5 V is applied at the second set of inputs (VINP2, VINN2). The cell is powered by a 5 V voltage and a 1 mA current source. Figure 6 shows that for an amplitude of 20 mV, the translation is performed only around the carrier frequency of 1 MHz.

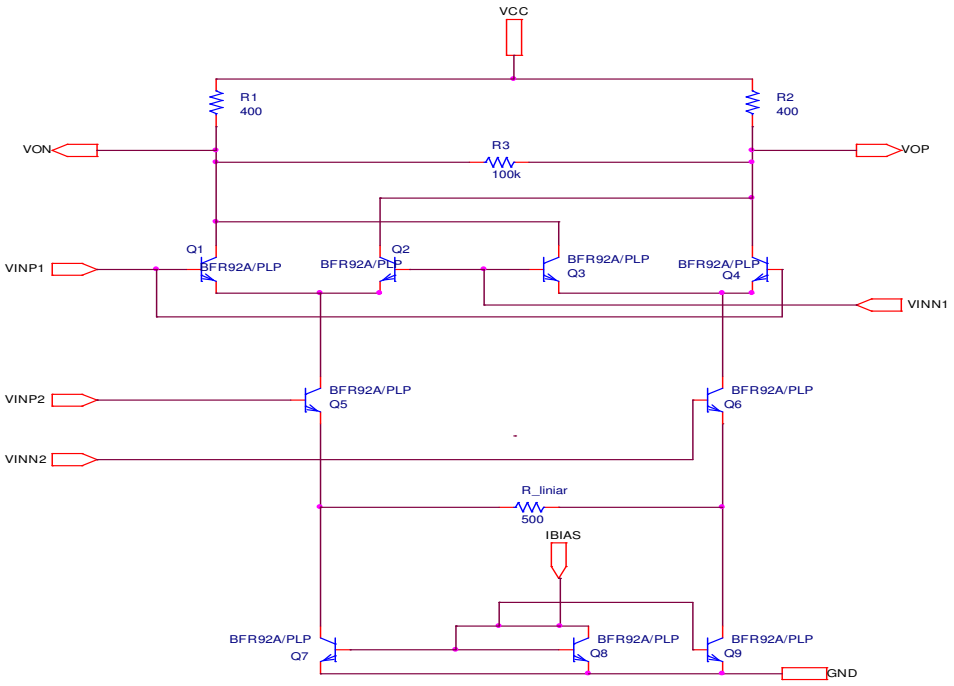

Fig.5. Multiplier circuit

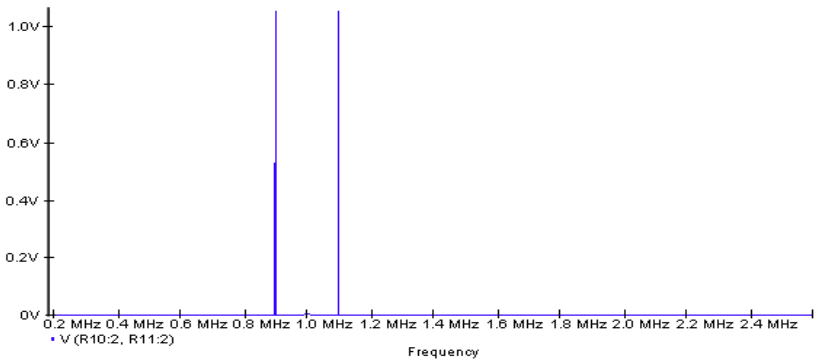

Fig. 6. The spectrum of the signal provided at the output of the multiplier (amplitude signal 20mV)

In order evaluate the performance of the Gilbert cell, a signal frequency of 1 MHz and an amplitude of 20 mV overlapped with a common mode voltage of 3 V is applied at the first set of inputs (VINP1, VINN1).

4.2. PEAK DETECTOR

The main function of the peak detector circuits is to extract the input signal envelope. This operation can be

done by using peak detectors or average value detectors. Figure 7 presents the peak detector implemented using a comparator designed with the operational amplifier OPA 358, diode D and the group (C, Rdesc).

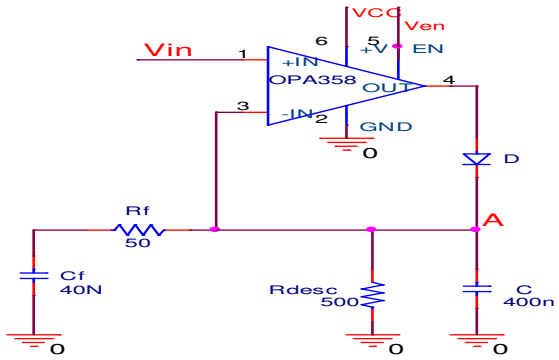

Fig.7. Peak detector circuit

In order to filter the signal obtained in node A a low-pass filter is implemented using the group (R_f, C_f). The operation of the circuit can be described as follows: initially, the capacitor C is discharged, so that the voltage applied to the positive input of the operational amplifier (V_{in}) is higher than the voltage applied at the input negative (V_A).

As long as the $V_{in}>V_A$ diode D conducts, the operational amplifier injects a current that charges the C capacitor. At a certain point, the voltage across the capacitor terminals (V_A) is equal to the input voltage. The comparator output then switches from 1 to 0 logical which causes the blocking of the diode D. Thus, the capacitor C begins to discharge through resistor R_{desc} with a time constant of $R \cdot C$. After this process, the voltage V_A becomes lower than the input voltage (V_{in}), and the cycle repeats itself.

If we want to detect the negative envelope of a signal, some changes must be made in the proposed peak detector circuit. First of all, the inversion of the diode D, the elimination of the current mirror designed with transistors Q_1 and Q_2, and its replacement with a constant current source whose main role is to inject current in the capacitor C_1. In order to evaluate the performance level of the peak detector circuit presented in Figure 7 a test signal amplitude modulated is used in the simulation environment. The harmonic modulator signal has a frequency of 25 kHz and an amplitude of 200 mV, and the carrier signal has a frequency of 1 MHz and an amplitude of 1V. The simulation results are presented in Figure 8.

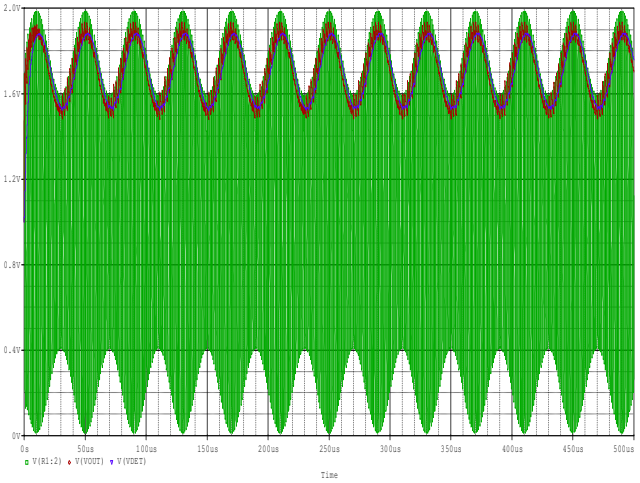

Fig.8 Peak detector operation in a time domain simulation

As can be noticed in Figure 8, the envelope detector follows the modulated signal peak amplitude ensuring a high performance level.

5. PERFORMANCE EVALUATION

In this section, the simulation results of the overall automatic gain controller circuit are presented. In order to simulate the proposed AGC circuit, an amplitude modulated signal (AM) is used, with the following characteristics: a carrier signal frequency of 1 MHz and an amplitude of 1V, with a harmonic modulated signal frequency of 25 kHz and an amplitude of 45 mV. Figure 9 presents the AM signal.

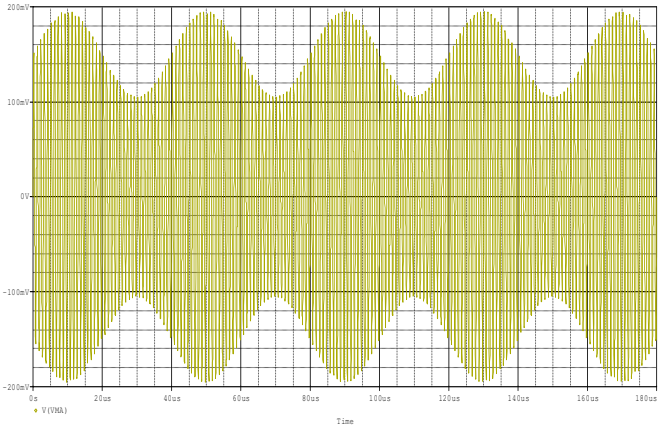

Fig.9. Amplitude Modulation test signal

After applying the test signal at the circuit's input and after performing a time analysis, the following results are obtained, as presented in Figure 10 and 11. The waveforms are obtained for an amplitude modulated input signal, where V_{set} =1.7 V and the linearization resistor R_liniar of the multiplier is set to 275 Ω.

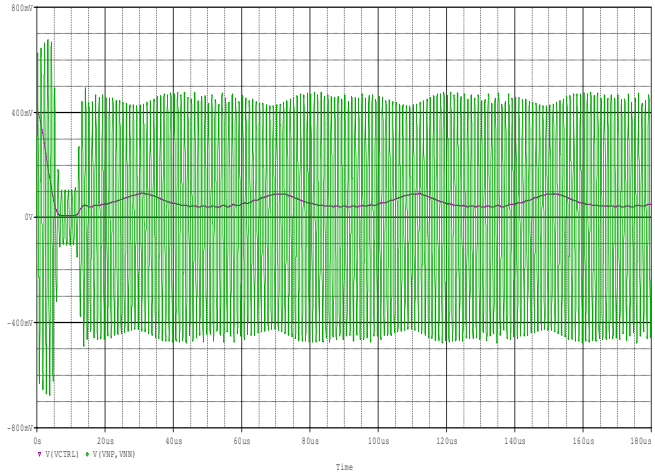

Fig. 10. The differential output signal (VNN, VPN) and the control signal (V_{ctrl})

The results obtained in the simulations reveal the existence of a transitory regime which lasts for about 17 us. After this transition regime, the output signal amplitude is approximately constant, as set by the reference voltage V_{set} 1.7 V, while the control signal V_{ctrl} ranges between 0 and 100 mV. Some errors may occur under these circumstances, caused by the transitory regime. The working frequency that the circuit has been tested is 1 MHz and the V_{set} reference voltage range can be adjusted within the 1.6 V- 2 V range.

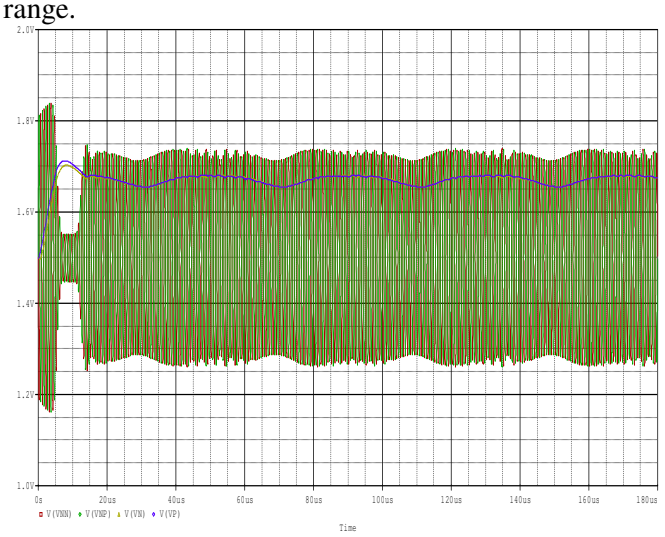

Fig. 11. The differential input signals (VNN, VPN) and the positive/negative envelops

6. CONCLUSIONS

Automatic gain control circuits are found in any system where a constant output signal must be obtained, regardless of the input signal variation. The complexity of these circuits is determined by the requirements of the communication system and therefore, the analysis, design and implementation can be difficult. The circuit presented in this paper is an AGC (automatic gain control) with feedback loop and can be implemented in a communication system. After verifying the operating principle of the system, the AGC is then implemented at a transistor level. The circuit operation and performance evaluation was analyzed for an amplitude modulated test signal.

The proposed circuit enables the adjustment of the amplitude level of the output signal by using an external V_{set} signal and is thus a cost effective solution. The work frequency is set at 1MHz.

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